# WAVEFORM GENERATION USING DAC 0080

# BY SUBATHRA S

This work is licensed under the Creative Commons Attribution-NonCommercial-Share Alike 2.5 India License. To view a copy of this license, visit http://creativecommons.org/licenses/by-nc-sa/2.5/in/deed.en or send a letter to Creative Commons, 171 Second Street, Suite 300, San Francisco, California, 94105, USA.

# WAVEFORM GENERATION USING DAC 0800

#### OBJECTIVE

To generate square waveform, triangular waveform, saw-tooth waveform and sine waveform using DAC 0800.

#### **APPARATUS REQUIRED**

- 8085 Microprocessor (ALS-SDA-85m) kit.
- Dual DAC Interface.
- Cathode Ray Oscilloscope.
- Flat Ribbon Cable.
- Power Supply (+5, +12v, -12v).

#### DESCRIPTION

The dual technology interface consists of two DACs the outputs of which are converted to voltages using Op-amps. The voltage outputs 0 to 10v or +/-5v of the Op-amps are terminated in a 4 way reliamate connector +0v external connection. A10v of stable voltage for DAC is obtained using LM723 regulator. A preset is provided to adjust the unipolar or bipolar output are selected by either J1 and J3 to J2 and J4 or by isolating the jumpers.

DAC 0800 is a monolithic. Its unique features are

- 1. Typical setting time of 100ns
- 2. If the full scale analog voltage in x volts, the smallest unit or the LSB  $(001)_2$  in equivalent to  $x/2^n$  volts. This is defined as resolution.
- 3. The MSB represents half of full scale value. i.e.  $MSB(100)_2 = x/2$  volt, assuming 3bit DAC.
- 4. For full scale, output is equal to the value of the full-scale input minus the value of 1 LSB input signal.

Full scale output = Full scale value - 1 LSB

- 5. Has complementary current outputs.
- 6. Has two quadrant wide range multiplying capacity.
- 7. Different output voltage of 20  $V_{pp}$  with simple resistor load.

#### DESIGN

DAC interface section comprises of (NOT in NIFC-06)

1. Input/ Output Decoding

The IC decoder 74LS138 and a NAND gate 74LS00, form the address decoding logic with address C0H, DAC1 is selected and with C8H DAC2 is selected.

2. DAC Conversion Circuit

DAC Conversion Circuit comprises 74LS273 latch, DAC 0800 and I to V convertor. The 8-bit data on the data bus is input to DAC0800, which gives the equal and complementing current output. The output voltage varies in steps of 10/256 = 40mV.

#### **INSTALLATION PROCEDURE**

1. Connect P3 in 85m to the connected C1 on the interface using a 26 core flat cable. Care should be taken that pin 1 of P3 on the kit coincides with pin1 of the cable. Observe the notch on the cable connector.

2. Power connections:

Connect +5/+12v/-12v to the interface color codes of power connectors on the interface

+5 - Orange/Blue /White

- GND Black
- +12v Red
- -12v Green.

#### PROBLEM ANALYSIS

#### SQUARE WAVEFORM GENERATION

With  $00_H$  as input to DAC, analog output is -5v and with FF<sub>H</sub> as input, the output is +5v. Input 00H and FF<sub>H</sub> at regular intervals, to generate a square wave. The frequency can be varied by varying the time delay.

#### TRIANGULAR WAVEFORM GENERATION

By outputing digital data from  $00_H$  to FF<sub>H</sub> in steps of  $01_H$  and then from FF<sub>H</sub> to  $00_H$ . Decrementing in steps of  $01_H$ , the triangular waveform is generated.

#### SINE WAVEFORM GENERATION

A look up table is formed and data are output continuously to DAC, from lookup table.  $\alpha = 128 + 128 \sin \theta$  where  $\theta = -90$  degree to +90 degree.



#### **CONTROL WORD 8255 PPI**



# CIRCUT DIAGRAM OF DUAL DAG IN INFC-06 (or INFC-07)



# SQUARE WAVEFORM GENERATION

#### ALGORITHM

1.Intialization a control word for 8255, for it to operate in I/O mode and for ports A, B and C to operate in output mode.

- 2.Clear the accumulator content and output it.
- 3.Call delay subroutine.
- 4. More immediate accumulator with  $FF_H$  and output it.
- 5.Continue the steps 2 to 4.

# ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
C800		MVI A,80 <sub>H</sub>	3E 80
C802		OUT CWR	D3 DB
C804	REPEAT	MVI A, OO <sub>H</sub>	3E 00
C806		OUT PORTA	D3 D8
C808		CALL DELAY	CD 15 C8
C80B		MVI A, FF <sub>H</sub>	3E FF
C80D		OUT PORTA	D3 D8
C80F		CALL DELAY	CD 15 C8
C812		JMP REPEAT	C3 04 C8
C815	DELAY	MVI C,85 <sub>H</sub>	0E 85
C817	AGAIN	DCR C	0D
C818		JNZ AGAIN	C2 17 C8
C81B		RET	C9

LABEL	MNEMONICS				DESCRI	PTION			
	MVI A,80 <sub>H</sub>	Initializing	the p	ort	s of th	ne PPI	8255 as	s O/P p	orts by
		writing the co	writting the control word as $\delta U_{\rm H}$ .						
		DATA D7	DATA $D_7$ $D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$						
		BITS 1	BITS 1 0 0 0 0 0 0 0						
		COMMENT I/O	COMMENT I/O Mode0 PortA PortC Mode0 PortB PortC						
		mode	mode O/P Upper O/P Lower						
		0/P 0/P							
		$80_{\rm H}$ is moved t	o acc	umu	lator.				
		REGISTE	RS						
		<b>A</b> 80 XX	F						
		B XX XX	C C						
		D XX XX	E T						
		H XX XX							
	OUT CWR	Control word	speci	fy	the I/O	functi	on for	each p	orts of
		8255.							
REPEAT	MVI A, OO <sub>H</sub>	Initialize por	rtA a	s 00	О <sub>н</sub> .				



	OUT PORTA	$FF_{H}$ is outputted thro portA. This is the ending of the
		square wavelorm.
		AMPLITUDE
		(v) T
		FF
		TIME PERIOD (MS)
	CALL	A delay is introduced for visibility of transmission.
	DELAY	
		AMPLITUDE
		(v)
		<-DELAY->
		FF
		00
		TIME PERIOSD (ms)
	JMP	The square waveform was generated continuously by
	REPEAT	repeating the cycle.
DELAY	MVI C,85 <sub>H</sub>	DELAY is a subprogram.
		Move 85 <sub>H</sub> to C register.
		REGISTERS
		$\begin{array}{c c} A & XX & XX & F \\ B & YX & \mathbf{P} \\ \end{array}$
		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
		$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
AGAIN	DCR C	$\begin{array}{c ccccc} A & & & & & \\ A & & & & & \\ B & & & & \\ M & & & & \\ D & & & & \\ H & & & & \\ XX & & & XX & \\ H & & & & \\ \end{array}$ $\begin{array}{c} F \\ C \\ E \\ H & & & \\ XX & & & \\ XX & & & \\ \end{array}$ $\begin{array}{c} F \\ C \\ E \\ H & & \\ XX & & \\ \end{array}$
AGAIN	DCR C	$\begin{array}{c c} A & \hline XX & XX \\ B & \hline XX & 85 \\ D & \hline XX & XX \\ H & \hline XX & XX \\ \end{array} \\ \hline \\ \hline$
AGAIN	DCR C JNZ AGAIN	$\begin{array}{c cccc} A & \hline XX & XX & F \\ B & \hline XX & 85 & C \\ D & \hline XX & XX & E \\ H & \hline XX & XX & L \\ \end{array}$ Decrement the C register content one by one in each step. Jump on no Zero(Z=0). If C register content is not equal to zero, then go on
AGAIN	DCR C JNZ AGAIN	A XX XX B XX 85 D XX XX H XX XX C D XX XX H XX XX L Decrement the C register content one by one in each step. Jump on no Zero(Z=0). If C register content is not equal to zero, then go on looping If C register content is equal to zero then
AGAIN	DCR C JNZ AGAIN	A XX XX B XX 85 D XX XX H XX XX E D Decrement the C register content one by one in each step. Jump on no Zero(Z=0). If C register content is not equal to zero, then go on looping. If C register content is equal to zero then come out of the loop(AGAIN) & continue sequentially.
AGAIN	DCR C JNZ AGAIN	A XX XX B XX 85 D XX XX H XX XX E L Decrement the C register content one by one in each step. Jump on no Zero(Z=0). If C register content is not equal to zero, then go on looping. If C register content is equal to zero then come out of the loop(AGAIN) & continue sequentially. REGISTERS
AGAIN	DCR C JNZ AGAIN	A XX XX A XX XX B XX 85 D XX XX H XX XX C D XX XX L Decrement the C register content one by one in each step. Jump on no Zero(Z=0). If C register content is not equal to zero, then go on looping. If C register content is equal to zero then come out of the loop(AGAIN) & continue sequentially. REGISTERS A XX XX F
AGAIN	DCR C JNZ AGAIN	A $XX XX XX F B XX 85 CD XX XX E H XX XX LDecrement the C register content one by one in eachstep.Jump on no Zero(Z=0).If C register content is not equal to zero, then go onlooping. If C register content is equal to zero thencome out of the loop(AGAIN) & continue sequentially.REGISTERSA XX XX FB XX 00 C$
AGAIN	DCR C JNZ AGAIN	A $XX XX XX F$ B $XX 85$ C D $XX XX E$ H $XX XX L$ Decrement the C register content one by one in each step. Jump on no Zero(Z=0). If C register content is not equal to zero, then go on looping. If C register content is equal to zero then come out of the loop(AGAIN) & continue sequentially. <b>REGISTERS</b> A $XX XX F$ B $XX 00$ C D $XX XX E$
AGAIN	DCR C JNZ AGAIN	A $XX XX XX F$ B $XX 85$ C D $XX XX E$ H $XX XX$ L Decrement the C register content one by one in each step. Jump on no Zero(Z=0). If C register content is not equal to zero, then go on looping. If C register content is equal to zero then come out of the loop(AGAIN) & continue sequentially. <b>REGISTERS</b> A $XX XX F$ B $XX 00$ C D $XX XX E$ H $XX XX$ L
AGAIN	DCR C JNZ AGAIN	A $\overrightarrow{XX}$ $\overrightarrow{XX}$ $\overrightarrow{XX}$ $\overrightarrow{F}$ B $\overrightarrow{XX}$ $\overrightarrow{XX}$ $\overrightarrow{F}$ D $\overrightarrow{XX}$ $\overrightarrow{XX}$ $\overrightarrow{E}$ H $\overrightarrow{XX}$ $\overrightarrow{XX}$ $\overrightarrow{L}$ Decrement the C register content one by one in each step.Jump on no Zero(Z=0).If C register content is not equal to zero, then go on looping. If C register content is equal to zero then come out of the loop(AGAIN) & continue sequentially. <b>REGISTERS</b> A $\overrightarrow{XX}$ $\overrightarrow{XX}$ B $\overrightarrow{XX}$ $\overrightarrow{C}$ D $\overrightarrow{XX}$ $\overrightarrow{XX}$ H $\overrightarrow{XX}$ $\overrightarrow{XX}$ L

### TRIANGULAR WAVEFORM GENERATION

#### ALGORITTHM

1.Intialization a control word for 8255,for it to operate in I/O mode and for ports A, B and C to operate in output mode.

2.Clear the accumulator content and output it.

3.Increment accumulator content and compare with  $FF_{H}$ 

4.Jump if nor zero to step 2.

5.Decrement accumulator content.

6.Output it and compare with  $00_{H}$  and go to step5 if not zero.

7.Continue the above steps.

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
C500		MVI A,80 <sub>h</sub>	3E 80
C502		OUT CWR	D3 DB
C504	START	MVI A, OO <sub>H</sub>	3E 00
C506	POS	OUT PORTA	D3 D8
C508		INR A	3C
C509		CPI FF <sub>H</sub>	FE FF
C50B		JNZ POS	C2 06 C5
C50E	NEG	DCR A	3D
C50F		OUT PORTA	D3 D8
C511		CPI 00 <sub>H</sub>	FE 00
C513		JNZ NEG	C2 0E C5
C516		JMP START	C3 04 C5

#### **ASSEMBLY LANGUAGE PROGRAM**

LABEL	MNEMONICS					DESCRI	PTION			
	MVI A,80 <sub>H</sub>	Initializ	ing th	ne p	ort	s of th	ne PPI	8255 as	5 0/P p	orts by
		writing t	che cor	ntro	l wo	ord as	80 <sub>H</sub> .			
		DATA	D <sub>7</sub>	D <sub>6</sub>	$D_5$	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		BITS	1	0	0	0	0	0	0	0
		COMMENT	I/O	Мос	de0	PortA	PortC	Mode0	PortB	PortC
			mode			O/P	Upper		O/P	Lower
							O/P			O/P
		80 <sub>H</sub> is mor	ved to	acc	cumu	lator.				
		REG	SISTERS	3						
		A 8	O XX	F						
		ВХ	XX XX	С						
		D X	XX XX	E						
		НХ	XX XX	L						
			1		6	-1 - T / O	<u> </u>	6	1	
	OUT CWR	Control v	vord sp	pecı	tγ	the I/O	functi	on for	each p	orts of
		8255.								









# SAWTOOTH WAVEFORM GENERATION

#### ALGORITHM

1.Intialization a control word for 8255, for it to operate in I/O mode and for ports A,B and C to operate in output mode.

2. Clear the accumulator content and output it.

3.Increment accumulator content and compare with FF<sub>H.</sub>

4.Jump if nor zero to step 2.

5.Continue the above steps.

# ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
C600		MVI A,80 <sub>H</sub>	3E 80
C602		OUT CWR	D3 DB
C604	START	MVI $A, OO_H$	3E 00
C606	REPEAT	OUT PORTA	D3 D8
C608		INR A	3C
C609		CPI FF <sub>H</sub>	FE FF
C60B		JNZ REPEAT	C2 06 C6
C60E		MVI A,00 <sub>H</sub>	3E 00
C610		OUT PORTA	D3 D8
C612		JMP START	C3 04 C6

LABEL	MNEMONICS	DESCRIPTION							
	MVI A,80 <sub>H</sub>	Initializing	the p	ports of	the PPI	8255	as O/P	ports	by
		writing the	contro	l word a	as 80 <sub>H</sub> .				
		DATA D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub>	$D_2$	$D_1$	D <sub>0</sub>	

		BITS COMMENT	1 I/O	0 0 Mode0	0 PortA	0 PortC	0 Mode0	0 PortB	0 PortC
			mode		O/P	Upper O/P		O/P	Lower O/P
		80 <sub>H</sub> is mov REG A 8 B X D X H X	o XX X XX X XX X XX X XX X XX	accumu 5 C E L	lator.				
START	OUT CWR MVI A, OO <sub>H</sub>	CWR speci Initializ	fy the	e I/O fu cA as 00	unction	for ea	ch port	s of 82	255.
		REG A 0 B X D X H X	O         XX           X         XX           X         XX           X         XX           X         XX           X         XX	5 F C E L					
REPEAT	OUT PORTA	$00_{\rm H}$ is ou of the sa	tputte wtooth	ed throm n wavefo	ugh por orm.	tA. Thi	is is t	he bas	e point
		AMPLITUDE (V) FF							
		00	•			TIME PE	RIOD (m	.s)	
	INR A	Increment generatin <b>REG</b> <b>A</b> D X H X AMPLITUDE (V)	The g the <b>ISTERS</b> <b>1</b> XX X XX X XX X XX F	accum slope o F C E L	ulator of the	conter sawtoot	nt. Th h wavef	is he	lps in
		0	$\begin{bmatrix} 1\\ 0 \end{bmatrix}$						
			-,			TIME	PERIOD	(ms)	
	CPI FF <sub>H</sub>	Compare I If accumu otherwise	mmedia lator Z fla	ately th content ag is re	ne accu t equal eset.	mulator to FF <sub>H</sub>	conten then Z	t with flag i	FF <sub>H.</sub> s set,





# SINE WAVEFORM GENERATION

#### ALGORITHM

1.Intialization a control word for 8255, for it to operate in I/O mode and for ports A, B and C to operate in output mode.

2.Intialize the HL register pair.

3. Move memory content to accumulator and output ir

4. Increment the HL register pair content. Decrement C register content.

5.Jump if no zero to step3 and move 24 into C register .

6.Decrement the content of HL register pair.

7. Move memory content to accumulator and output it.

8.Decrement it and compare with zero. If no zero jump to step6.

9.Continue the above steps.

# ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
C300		MVI A,80 <sub>H</sub>	3E 80
C302		OUT CWR	D3 DB
C304	START	MVI C,24 <sub>H</sub>	0E 24
C306		LXI H,C900 <sub>H</sub>	21 00 C4
C309	POS	MOV A,M	7E
C30A		OUT PORTA	D3 D8
C30C		INX H	23
C30D		DCR C	0D
C30E		JNZ POS	C2 09 C3
C311		MVI C,24 <sub>H</sub>	0E 24
C313	NEG	DCX H	2B
C314		MOV A,M	7E
C315		OUT PORTA	D3 D8
C317		DCR C	0D
C318		JNZ NEG	C2 13 C3
C31B		JMP START	C3 04 C3

LABEL	MNEMONICS			DESCRIPTION						
	MVI A,80 <sub>H</sub>	Initializ	ing the	port	ts c	of the PPI	8255 as	0/P por	ts by	writing
		the contr	ol word a	as 8	О <sub>н</sub> .					
		DATA	D <sub>7</sub>	D <sub>6</sub>	$D_5$	D <sub>4</sub>	D <sub>3</sub>	$D_2$	$D_1$	D <sub>0</sub>
		BITS	1	0	0	0	0	0	0	0
		COMMENT	I/0	Мос	de0	PortA	PortC	Mode0	PortB	PortC
			mode			0/P	Upper		0/P	Lower
						- /	O/P		- /	O/P
							- /			- /
		80. is mov	ved to ac	cumu	ılat	or.				
		REG	ISTERS							
		A 8	0 XX F							
		BV	v vv C							
		D V	V VV E							
		H V	V VV L							
	OUT CWR	Control w	ord speci	fy	the	I/O funct	ion for ea	ich port	ts of 8	255.
START	MVI C,24 <sub>H</sub>	Initializ	e C regis	ster	as	24 <sub>H</sub> .				
		REG	ISTERS							
		A 8	0 XX F							
		ВХ	X 24 C							
		DX	X XX E							
		Н Х	X XX L							
			]							
		Setting c	count for	100	ok ι	up table d	lata seque	nce i.e	. 24 da	ata are
		loaded f	rom memo	ry	for	sine way	veform gen	eration	n in p	ositive
		direction								
	LXI	Initializ	e the me	emor	у р	ointer at	C900 <sub>H</sub> .i.	e. loa	ds the	16-bit
	Н,С900 <sub>н</sub>	data in t	he regist	ler	pai	r designat	ed.			
		REG	ISTERS							
		A 8	0 XX F							
		ВХ	X 24 C							
		DX	X XX E							
		нс	9 00 <sup>L</sup>							
		0000 i .	- h					1 -1		
		$C900_{\rm H}$ IS	leek we t	y p	OTU	ter to the	e starting	addres	S OI L	ne sine
		waveloliii	TOOK UP (	api	e ua	ata sequen	ce.			
		C900				• .				
		C901	00	НГ	mer	mory point	er			
		C902	01							
		C903	02							
		C 904	04							
		0,001	08							
POS	MOV A.M	Memory po	inter cor	iten	t 00	O <sub>u</sub> is moved	to accum	ilator		
100	110 V 11,11	REG	ISTERS	reen		OH ID MOVEC		aracor.		
		A 0	0 XX F							
		B V	x 24 C							
		H C								
			2 UU E							
	OUT PORTA	00 <sub>H</sub> is ou	atputted	thr	ouat	n portA.	This is t	he bea	inning	of the
		sine wave	form in a	oosi	tiv	e directio	on .i.e.Sto	orina ti	he accu	mulator
		content i	n the DAG	da da	ta i	latches.				

	AMPLITUDE (v) FF 00 TIME PERIOD (ms)
INX H	Increment the HL register pair by 1.The instruction views the contents of the HL registers as a 16-bit number. No flags are affected.           REGISTERS         A       00 XX       F         B       XX       24       C         D       XX       XX       E         H       C9 01       L       C         C901_H is the memory pointer of the sine waveform look up table data sequence.       MEMORY         C900       00       01       HL memory pointer         C901       02       02       02         C903       04       08       HL memory pointer
DCR C	Decrement the C register content one by one in each step. <b>REGISTERS</b> A 00 XX F B XX 23 C D XX XX E H C9 01 L
JNZ POS MVI C,24 <sub>H</sub>	Jump on no Zero(Z=0). If C register content is not equal to zero, then go on looping. If C register content is equal to zero then come out of the loop(POS) & continues sequentially. <b>REGISTERS</b> A FF XX F B XX <b>00</b> C D XX XX E H C9 23 L Reinitialize C register as 24 <sub>H</sub> .





# LOOK UP TABLE

ALPHA = 128 + 128 SIN (THETA) Where THETA = -90 degree to +90 degree for every 5 degree.

ADDRESS	ANGLE	DEGREE	HEX CODE	DATA
				(HEX CODE
				Approximate)
C900	-90	0.0	00	00
C901	-85	0.48	00	01
C902	-80	1.94	01	02
C903	-75	4.36	04	04
C904	-70	7.719	08	08
C905	-65	11.99	0B	11
C906	-60	17.14	11	17
C907	-55	23.14	17	1E
C908	-50	29.94	1D	25
C909	-45	37.49	25	2D
C90A	-40	45.72	2E	36
С90В	-35	54.58	37	40
C90C	-30	64.00	40	49
C90D	-25	73.90	4A	54

C90E	-20	84.22	54	5E
C90F	-15	94.87	5F	69
C910	-10	105.77	6A	74
C911	-05	116.84	74	7F
C912	00	128.00	80	84
C913	05	139.15	8B	95
C914	10	150.20	96	9F
C915	15	161.12	A1	AF
C916	20	171.77	A6	B4
C917	25	182.09	В6	CO
C918	30	192.00	C0	C8
C919	35	201.42	С9	DO
C91A	40	210.27	D2	D8
C91B	45	218.50	DA	ΕO
C91C	50	226.05	E2	EA
C91D	55	232.85	E8	ED
C91E	60	238.85	EE	EF
C91F	65	244.00	F4	F2
C920	70	248.28	F8	F9
C921	75	251.63	FB	FC
C922	80	254.05	FE	FD
C923	85	255.51	FF	FF
C924	90	256.00	100	00

#### TIPS

IC	ADDRESS			
	PORT A	PORT B	PORT C	CONTROL
PPI 8255 (U4)	D8	D9	DA	DB
PPI 8255 (U3)	FO	Fl	F2	F3

# OBSERVATION

WAVEFORM	AMPLITUDE (V)	TIME PERIOD (ms)	FREQUENCY (Hz)
SQUARE	0.001	0.6	1.67
TRIANGLE	4.4	1.3	0.77
SAWTOOTH	1.1	2.6	0.38
SINE	1.0	0.88	1.14

#### VERIFICATION

Check the waveform at the output lines of the 8255. The frequency of the waveform depends solely on the time delay routine used.

#### REFERENCE

1. Ramesh S.Gaonkar, Microprocessor Architecture, Programming, and Applications, Fourth Edition, Penram International Publishing (India), 2000.

- 2. S.Subathra, Advanced Microprocessor Lab, Record work, Adhiparashakthi Engineering College, Melmaruvathur, October 2002
- 3. S.Subathra, "Programming in 8085 Microprocessor and its applications An Innovative Analysis", Technical Report, Adhiparashakthi Engineering College, Melmaruvathur, March 2003
- 4. Micro-85 EB, User Manual, Version 3.0, CAT #M85 EB-002, VI Microsystems Pvt. Ltd., Chennai.