

STONE GENERATOR

BY
SUBATHRA S

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TONE GENERATOR

AIM

To write an assembly language program to generate tones using software.

APPARATUS REQUIRED

- 8085 Microprocessor Trainer kit
- Flat Ribbon Cable
- Tone generator kit
- Power Supply

DESCRIPTION

Tone generator is a circuit which generates different tones depending on the input signal and its frequency. This circuit contains AND gates (IC is 74HC102). The two inputs for AND gates are one from 8255 (26 core FRC cable connected to P3) and other input is from 8253 IC on the kit. With the help of FRC, we can connect this signal from p2 on the kit to JP2 on the interface. These input signals are modulated and outputted to the transistor Q1 whose collector current varies depending on the base current fed by the O/P of the AND gate, this variation in collector current causes the speaker diaphragm to vibrate at different frequencies and hence to output various tones.

The user can write various programs to generate different tones to the output of speaker.

On the interface one beared speaker is mounted and also to work under silent areas headphone socket is provided in addition to this, a volume control pot R6(500 ohm) provided to vary the volume of the output.

Steps to be followed to generate tone using software

Calculate the Hexa count to be loaded to 8253 16 bit counter for the particular frequency of the required time. Using the formula,

$$\text{Count (dec)} = 1.5 \text{ MHz} / (\text{frequency required})$$

After this convert the count in decimal value to Hex value & load 16 bit data to 8253 counts. In hardware of the interface when you connect FRC clock1 of 8253 is shorted to clock2 of the same on the kit, at clock2 you have 1.5MHz of the frequency.

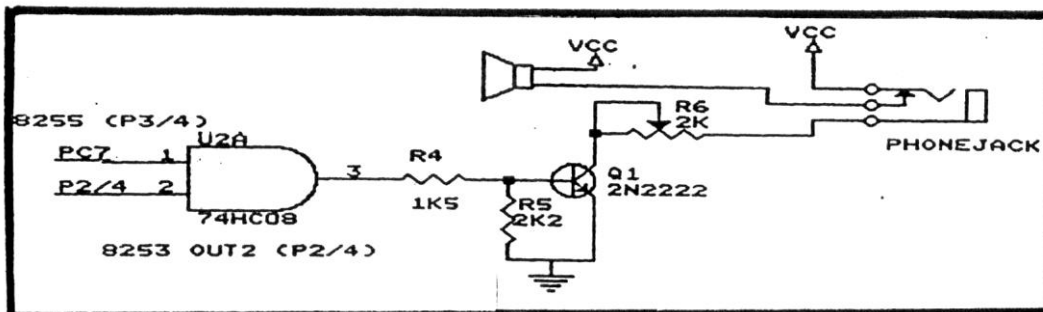
- a) Disable the output of AND gate by sending '0' to PC7
- b) Enable the same by sending 1 to PC7
- c) Call different delays to generate tones for that particular duration
- d) Disable AND gate output and call delay in order to give pause between tones
- e) Load next 16 bit hex data to 8253 counter and repeat the above steps

Some of the fundamental frequencies are given below

TONE NAME	OCTAVE 0	OCTAVE 1	OCTAVE 2	OCTAVE 3
Sa	130.810	261.630	523.250	1046.500
Re	146.830	293.660	587.330	1174.700
Ga	164.810	329.630	659.260	1318.500
Ma	174.610	349.230	698.460	1396.900

Pa	196.000	392.000	784.000	1568.000
Dha	220.000	440.000	880.000	1760.000
Ni	246.940	493.883	987.770	1975.540

CIRCUIT DIAGRAM



TO WORK WITH TONE GENERATOR

- a) In addition to the FRC connected from P3 of kit to JP1 on interface(26 pin). Connect one more FRC connect P2 (20 pin) on the kit to JP2(20 pin) on the interface.
- b) Connect +5 & GND to generate low, execute the program as GO <starting address> <EXEC> . Now you can hear music (or tone) at the output of the speaker depending on your program. The tone volume can be controlled by varying R6 pot mounted on the interface.

If you connect head phone externally to jack provided the on board speaker is disabled and you will get the output on head phone.

FUNDAMENTAL FREQUENCY OCTAVE — 1

- SA = 1.5 Mhz / 261.630 = 5740.5 = 5741_d = 166D_H
- RE = 1.5 Mhz / 293.660 = 5107.9 = 5108_d = 13F4_H
- GA = 1.5 Mhz / 329.630 = 4550.5 = 4551_d = 11C7_H
- MA = 1.5 Mhz / 349.230 = 4295.1 = 4295_d = 10C7_H
- PA = 1.5 Mhz / 392.000 = 3826.5 = 3827_d = 0EF3_H
- DHA = 1.5 Mhz / 440.000 = 3409.09 = 3409_d = 0D51_H
- NI = 1.5 Mhz / 493.883 = 3037.15 = 3037_d = 0BDD_H

ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
C100		MVI A,80 _H	3E 80
C102		OUT CWR	D3 DB
C104		MVI A,B6 _H	3E B6
C106		OUT TIMERCTRL	D3 CB
C108	REPEAT	MVI B,07 _H	06 07
C10A		LXI H,C200 _H	21 00 C2

C10D	NEXT	MVI A,M	7E
C10E		OUT TIMER2	D3 CA
C110		INX H	23
C111		MOV A,M	7E
C112		OUT TIMER2	D3 CA
C114		MVI A,80 _H	3E 80
C116		OUT PORTC	D3 DA
C118		CALL DELAY	CD 27 C1
C11B		MVI A,00 _H	3E 00
C11D		OUT PORTC	D3 DA
C11F		INX H	23
C120		DCR B	05
C121		JNZ NEXT	C2 OD C1
C124		JMP REPEAT	C3 08 C1
C127	DELAY	MVI C,04 _H	0E 04
C129	START	LXI D,FFFF _H	11 FF FF
C12B	LOOP1	DCX D	1B
C12C		MOV A,E	7B
C12D		ORA D	B2
C12E		JNZ LOOP1	C2 2B C1
C131		DCR C	0D
C132		JNZ START	C2 29 C1
C135		RET	C9

PROGRAM TRACE

LABEL	MNEMONICS	DESCRIPTION																																													
	MVI A,80 _H	<p>Initializing the ports of the PPI 8255 as O/P ports by writing the control word as 80_H.</p> <table border="1"> <tr> <td>DATA</td> <td>D₇</td> <td>D₆</td> <td>D₅</td> <td>D₄</td> <td>D₃</td> <td>D₂</td> <td>D₁</td> <td>D₀</td> </tr> <tr> <td>BITS</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>COMMENT</td> <td>I/O mode</td> <td>Mode0</td> <td>PortA O/P</td> <td>PortC Upper O/P</td> <td>Mode0</td> <td>PortB O/P</td> <td>PortC Lower O/P</td> <td></td> </tr> </table> <p>80_H is moved to accumulator.</p> <p>REGISTERS</p> <table border="1"> <tr> <td>A</td> <td>80</td> <td>XX</td> <td>F</td> </tr> <tr> <td>B</td> <td>XX</td> <td>XX</td> <td>C</td> </tr> <tr> <td>D</td> <td>XX</td> <td>XX</td> <td>E</td> </tr> <tr> <td>H</td> <td>XX</td> <td>XX</td> <td>L</td> </tr> </table>	DATA	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	BITS	1	0	0	0	0	0	0	0	COMMENT	I/O mode	Mode0	PortA O/P	PortC Upper O/P	Mode0	PortB O/P	PortC Lower O/P		A	80	XX	F	B	XX	XX	C	D	XX	XX	E	H	XX	XX	L		
DATA	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																																							
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	OUT CWR	Control word specifies the I/O function for each port of 8255.																																													
	MVI A,B6 _H	<p>Initializing the COUNTER 2 of the PIT 8253 in MODE 3 by writing the control word as B6_H.</p> <table border="1"> <tr> <td>COMMENT</td> <td colspan="2">SELECT COUNTER</td> <td colspan="2">READ/LOAD</td> <td colspan="3">MODE</td> <td>BCD/BINARY COUNT</td> </tr> <tr> <td></td> <td>SC1</td> <td>SC0</td> <td>RL1</td> <td>RL0</td> <td>M2</td> <td>M1</td> <td>M0</td> <td></td> </tr> <tr> <td>DATA</td> <td>D₇</td> <td>D₆</td> <td>D₅</td> <td>D₄</td> <td>D₃</td> <td>D₂</td> <td>D₁</td> <td>D₀</td> </tr> <tr> <td>BITS</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>OBSERVE</td> <td colspan="2">COUNTER 2</td> <td colspan="2">LSB/MSB</td> <td colspan="3">MODE 3</td> <td>BINARY COUNT</td> </tr> </table>	COMMENT	SELECT COUNTER		READ/LOAD		MODE			BCD/BINARY COUNT		SC1	SC0	RL1	RL0	M2	M1	M0		DATA	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	BITS	1	0	1	1	0	1	1	0	OBSERVE	COUNTER 2		LSB/MSB		MODE 3			BINARY COUNT
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A	B6	XX	F																									
B	XX	XX	C																									
D	XX	XX	E																									
H	XX	XX	L																									
	OUT TIMERCTRL	<p>Output it through TIMERCTRL.</p> <p><u>NOTE:</u></p> <ul style="list-style-type: none"> ❖ Opcode of TIMERCTRL is CB. 																										
REPEAT	MVI B,07_H	<p>Initialize B register with number of count.</p> <p>REGISTERS</p> <table border="1"> <tr> <td>A</td> <td>XX</td> <td>XX</td> <td>F</td> </tr> <tr> <td>B</td> <td>07</td> <td>XX</td> <td>C</td> </tr> <tr> <td>D</td> <td>XX</td> <td>XX</td> <td>E</td> </tr> <tr> <td>H</td> <td>XX</td> <td>XX</td> <td>L</td> </tr> </table>	A	XX	XX	F	B	07	XX	C	D	XX	XX	E	H	XX	XX	L										
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	LXI H,C200_H	<p>Initialize the memory pointer at C200_H .i.e. loads the 16-bit data in the register pair designated.</p> <p>REGISTERS</p> <table border="1"> <tr> <td>A</td> <td>XX</td> <td>XX</td> <td>F</td> </tr> <tr> <td>B</td> <td>07</td> <td>XX</td> <td>C</td> </tr> <tr> <td>D</td> <td>XX</td> <td>XX</td> <td>E</td> </tr> <tr> <td>H</td> <td>C2</td> <td>00</td> <td>L</td> </tr> </table> <p>C200_H is the memory pointer.</p> <p>MEMORY</p> <table border="1"> <tr> <td>C200</td> <td>CB</td> </tr> <tr> <td>C201</td> <td>2C</td> </tr> <tr> <td>C202</td> <td>E7</td> </tr> <tr> <td>C203</td> <td>27</td> </tr> <tr> <td>C204</td> <td>8D</td> </tr> </table>	A	XX	XX	F	B	07	XX	C	D	XX	XX	E	H	C2	00	L	C200	CB	C201	2C	C202	E7	C203	27	C204	8D
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NEXT	MVI A,M	<p>LSB of 'Sa' is loaded in to accumulator.</p> <p>REGISTERS</p> <table border="1"> <tr> <td>A</td> <td>CB</td> <td>XX</td> <td>F</td> </tr> <tr> <td>B</td> <td>XX</td> <td>XX</td> <td>C</td> </tr> <tr> <td>D</td> <td>XX</td> <td>XX</td> <td>E</td> </tr> <tr> <td>H</td> <td>XX</td> <td>XX</td> <td>L</td> </tr> </table>	A	CB	XX	F	B	XX	XX	C	D	XX	XX	E	H	XX	XX	L										
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B	XX	XX	C																									
D	XX	XX	E																									
H	XX	XX	L																									
	OUT TIMER2	<p>CB_H is outputted thro TIMER2.</p> <p><u>NOTE:</u></p> <ul style="list-style-type: none"> ❖ Opcode of TIMER2 is CA. 																										
	INX H	<p>Increment the HL register pair by 1.The instruction views the contents of the HL registers as a 16-bit number. No flags are affected.</p>																										

		<p align="center">REGISTERS</p> <table border="1"> <tr><td>A</td><td>CB</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>07</td><td>XX</td><td>C</td></tr> <tr><td>D</td><td>XX</td><td>XX</td><td>E</td></tr> <tr><td>H</td><td>C2</td><td>01</td><td>L</td></tr> </table> <p>C201_H is the memory pointer.</p> <p align="center">MEMORY</p> <table border="1"> <tr><td>C200</td><td>CB</td></tr> <tr><td>C201</td><td>2C</td></tr> <tr><td>C202</td><td>E7</td></tr> <tr><td>C203</td><td>27</td></tr> <tr><td>C204</td><td>8D</td></tr> </table> <div style="display: flex; align-items: center; margin-left: 100px;"> <div style="border: 1px solid black; padding: 2px 10px;">HL memory pointer</div> <div style="margin: 0 10px;">←</div> </div>	A	CB	XX	F	B	07	XX	C	D	XX	XX	E	H	C2	01	L	C200	CB	C201	2C	C202	E7	C203	27	C204	8D
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	MOV A,M	<p>MSB of 'Sa' is loaded in to accumulator.</p> <p align="center">REGISTERS</p> <table border="1"> <tr><td>A</td><td>2C</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>07</td><td>XX</td><td>C</td></tr> <tr><td>D</td><td>XX</td><td>XX</td><td>E</td></tr> <tr><td>H</td><td>C2</td><td>01</td><td>L</td></tr> </table>	A	2C	XX	F	B	07	XX	C	D	XX	XX	E	H	C2	01	L										
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	OUT TIMER2	2C _H is outputted thro TIMER2.																										
	MVI A,80_H	<p>Move 80_H immediately in to accumulator.</p> <p align="center">REGISTERS</p> <table border="1"> <tr><td>A</td><td>80</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>07</td><td>XX</td><td>C</td></tr> <tr><td>D</td><td>XX</td><td>XX</td><td>E</td></tr> <tr><td>H</td><td>C2</td><td>01</td><td>L</td></tr> </table>	A	80	XX	F	B	07	XX	C	D	XX	XX	E	H	C2	01	L										
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	OUT PORTC	<p>Initialize the ports.</p> <table border="1" style="width: 100%; text-align: center;"> <tr><td>DATA</td><td>PC₇</td><td>PC₆</td><td>PC₅</td><td>PC₄</td><td>PC₃</td><td>PC₂</td><td>PC₁</td><td>PC₀</td></tr> <tr><td>BITS</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> </table> <p>PC₇ =1 ,Enable AND gate output by sending 1 bit (high signal) to PC₇.</p>	DATA	PC ₇	PC ₆	PC ₅	PC ₄	PC ₃	PC ₂	PC ₁	PC ₀	BITS	1	0	0	0	0	0	0	0								
DATA	PC ₇	PC ₆	PC ₅	PC ₄	PC ₃	PC ₂	PC ₁	PC ₀																				
BITS	1	0	0	0	0	0	0	0																				
	CALL DELAY	Call delay sub program.																										
	MVI A,00_H	<p>Clear the accumulator.</p> <p align="center">REGISTERS</p> <table border="1"> <tr><td>A</td><td>00</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>07</td><td>XX</td><td>C</td></tr> <tr><td>D</td><td>XX</td><td>XX</td><td>E</td></tr> <tr><td>H</td><td>C2</td><td>01</td><td>L</td></tr> </table>	A	00	XX	F	B	07	XX	C	D	XX	XX	E	H	C2	01	L										
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	INX H	Increment the HL register pair by 1. REGISTERS <table border="1"> <tr><td>A</td><td>E7</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>07</td><td>XX</td><td>C</td></tr> <tr><td>D</td><td>XX</td><td>XX</td><td>E</td></tr> <tr><td>H</td><td>C2</td><td>02</td><td>L</td></tr> </table>	A	E7	XX	F	B	07	XX	C	D	XX	XX	E	H	C2	02	L
A	E7	XX	F															
B	07	XX	C															
D	XX	XX	E															
H	C2	02	L															
	DCR B	Decrease the count of B register since 'Sa' is obtained. REGISTERS <table border="1"> <tr><td>A</td><td>XX</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>06</td><td>XX</td><td>C</td></tr> <tr><td>D</td><td>XX</td><td>XX</td><td>E</td></tr> <tr><td>H</td><td>C2</td><td>02</td><td>L</td></tr> </table>	A	XX	XX	F	B	06	XX	C	D	XX	XX	E	H	C2	02	L
A	XX	XX	F															
B	06	XX	C															
D	XX	XX	E															
H	C2	02	L															
	JNZ NEXT	For single loop, to play sa, re, ga, ma, pa, dha, ni Jump to next.																
	JMP REPEAT	In order to play continuously the tune, repeat the process.																

DELAY	MVI C,04_H	Move 04 _H immediately to C register. REGISTERS <table border="1"> <tr><td>A</td><td>XX</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>XX</td><td>04</td><td>C</td></tr> <tr><td>D</td><td>XX</td><td>XX</td><td>E</td></tr> <tr><td>H</td><td>XX</td><td>XX</td><td>L</td></tr> </table>	A	XX	XX	F	B	XX	04	C	D	XX	XX	E	H	XX	XX	L										
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START	LXI D,FFFF_H	Initialize the memory pointer at FFFF _H .i.e. loads the 16-bit data in the register pair designated. REGISTERS <table border="1"> <tr><td>A</td><td>XX</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>XX</td><td>04</td><td>C</td></tr> <tr><td>D</td><td>FF</td><td>FF</td><td>E</td></tr> <tr><td>H</td><td>XX</td><td>XX</td><td>L</td></tr> </table> <p>FFFF_H is the memory pointer.</p> <p>MEMORY</p> <table border="1"> <tr><td>FFFF</td><td>XX</td></tr> <tr><td>FFFE</td><td>XX</td></tr> <tr><td>FFFD</td><td>XX</td></tr> <tr><td>FFFC</td><td>XX</td></tr> <tr><td>FFFB</td><td>XX</td></tr> </table>	A	XX	XX	F	B	XX	04	C	D	FF	FF	E	H	XX	XX	L	FFFF	XX	FFFE	XX	FFFD	XX	FFFC	XX	FFFB	XX
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FFFE	XX																											
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FFFB	XX																											
LOOP1	DCX D	Decrement the HL register pair by 1.The instruction views the contents of the HL registers as a 16-bit number. No flags are affected. REGISTERS <table border="1"> <tr><td>A</td><td>XX</td><td>XX</td><td>F</td></tr> <tr><td>B</td><td>XX</td><td>XX</td><td>C</td></tr> <tr><td>D</td><td>FF</td><td>FE</td><td>E</td></tr> <tr><td>H</td><td>XX</td><td>XX</td><td>L</td></tr> </table> <p>FFFE_H is the memory pointer.</p>	A	XX	XX	F	B	XX	XX	C	D	FF	FE	E	H	XX	XX	L										
A	XX	XX	F																									
B	XX	XX	C																									
D	FF	FE	E																									
H	XX	XX	L																									

		<p style="text-align: center;">MEMORY</p> <table style="border-collapse: collapse;"> <tr> <td style="padding: 2px;">FFFF</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td></td> </tr> <tr> <td style="padding: 2px;">FFFE</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="text-align: center;">← DE memory pointer</td> </tr> <tr> <td style="padding: 2px;">FFFD</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td></td> </tr> <tr> <td style="padding: 2px;">FFFC</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td></td> </tr> <tr> <td style="padding: 2px;">FFFB</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td></td> </tr> </table>	FFFF	XX		FFFE	XX	← DE memory pointer	FFFD	XX		FFFC	XX		FFFB	XX		
FFFF	XX																	
FFFE	XX	← DE memory pointer																
FFFD	XX																	
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	MOV A,E	<p>Move E register to accumulator.</p> <p style="text-align: center;">REGISTERS</p> <table style="border-collapse: collapse;"> <tr> <td style="padding: 2px;">A</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">FE</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="padding: 2px;">F</td> </tr> <tr> <td style="padding: 2px;">B</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="padding: 2px;">C</td> </tr> <tr> <td style="padding: 2px;">D</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="padding: 2px;">E</td> </tr> <tr> <td style="padding: 2px;">H</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="padding: 2px;">L</td> </tr> </table>	A	FE	XX	F	B	XX	XX	C	D	XX	XX	E	H	XX	XX	L
A	FE	XX	F															
B	XX	XX	C															
D	XX	XX	E															
H	XX	XX	L															
	ORA D	OR the accumulator content with D register content.																
	JNZ LOOP1	Jump if no zero to Labeled LOOP1.																
	DCR C	<p>Decrement the C register content.</p> <p style="text-align: center;">REGISTERS</p> <table style="border-collapse: collapse;"> <tr> <td style="padding: 2px;">A</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="padding: 2px;">F</td> </tr> <tr> <td style="padding: 2px;">B</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">03</td> <td style="padding: 2px;">C</td> </tr> <tr> <td style="padding: 2px;">D</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="padding: 2px;">E</td> </tr> <tr> <td style="padding: 2px;">H</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">XX</td> <td style="padding: 2px;">L</td> </tr> </table>	A	XX	XX	F	B	XX	03	C	D	XX	XX	E	H	XX	XX	L
A	XX	XX	F															
B	XX	03	C															
D	XX	XX	E															
H	XX	XX	L															
	JNZ START	Jump if no zero to Labeled START.																
	RET	Return to main program.																

EXECUTION

ADDRESS	STONE NAME	FREQUENCY (Hz)	HEXADECIMAL (hexa)
C200	Sa	261.630	1665 _H
C202	Re	293.660	13F4 _H
C204	Ga	329.630	11C7 _H
C206	Ma	349.230	10C7 _H
C208	Pa	392.000	0EF3 _H
C20A	Dha	440.000	0D57 _H
C20C	Ni	493.883	0BDD _H

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