PROGRAMMABLE INTERVAL TIMER INTERFACE



This work is licensed under the Creative Commons Attribution-NonCommercial-Share Alike 2.5 India License. To view a copy of this license, visit http://creativecommons.org/licenses/by-nc-sa/2.5/in/deed.en or send a letter to Creative Commons, 171 Second Street, Suite 300, San Francisco, California, 94105, USA.

PROGRAMMABLE INTERVAL TIMER INTERFACE

OBJECTIVE

To write an assembly language program to interface programmable interval timer with 8085 microprocessor trainer kit and observe its various modes.

APPARATUS REQUIRED

- 8085 Microprocessor Trainer Kit
- · Programmable interval timer interfacing kit
- Power Supply
- Flat Ribbon Cable

DESCRIPTION

The chip has a control register which stores the operational mode of each counter. This register can only be written into and no read operations of its contents are possible. Writing corresponding control word by simple I/O operation can individually program each counter of 8253.

CONTORL WORD FORMAT 8253

DA!	ГА	DESCRIPTION								
BI	Г									
D ₀	BCD	BIN	ARY/	BC	D					
D_1	M0	MOD	E							
		M2	M1	М	0 MC	DE				
D_2	M1	0	0	0	0					
		0	0	1	1					
		0	1	0	2					
D_3	M2	0	1	1	3					
		1	0	0	4					
		1	0	1	5					
D_4	RL0	REA	D/LC	AD						
		RL	l RI	01						
		0	0		Lat	ch				
D_5	RL1	0	1		LSB					
		1	0		MSB					
		1	1		LSB	/MSI	3			
D ₆	SC0	SEL	ECT	СО	UNTE	R				
		SCO) sc	21	CH#					
		0	0		0					
D ₇	SC1	0	1		1					
		1	0		2					
		1	1		Х					

INTERRUPT ON TERMINAL COUNT

ALGORITHM

1. The output will be low initially after mode set operation.

2. After loading the counter, the output will remain while counting.

3.On terminal count, output will go high until reloaded again.

4. After six clock pulses we can notice that the output goes high.

ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4100		MVI A, $30_{\rm H}$	3E 30
4102		OUT CWR	D3 CE
4104		MVI A,05 _h	3E 05
4106		OUT CNTO	D3 C8
4108		MVI A,00 _H	3E 00
410A		OUT CNTO	D3 C8
410C		HLT	76

LABEL	MNEMONICS		DESCRIPTION										
	MVI $A, 30_{H}$	Initializ	itializing the <code>COUNTER 0</code> of the PIT 8253 in <code>MODE 0</code> k										
		writing t	iting the control word as 30_{H} .										
		COMMENT	SELEC	Г	READ)/	MODE			BCD/			
			COUNTI	ER	LOAD)				BINARY			
			SC1	SC0	RL1	RL0	M2	M1	M0	COUNT			
		DATA	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D_1	D ₀			
		BITS	0	0	1	1	0	0	0	0			
		OBSERVE	C0UN	TER 0	LSB/	MSB	M	ODE	E 0	BINARY			
										COUNT			
		30 _H is mov	ved to	accumu	lator	•							
		REG	ISTERS	_									
		A 3	0 XX	F,									
		BX	X XX	C E									
		D X	X XX	Е т									
		п Х	X XX	Ц									
	OUT CWR	Write the	contr	ol word	lint	the c	ontr	olr	oris	tor			
		HINTS.	CONCL	OI WOIC			UTCL		Cyrc	JUCI.			
			ode us	ed for	CWR	is CE							
		\Box The	cont.	rol re	aiste	er is	". : nc	t 1	oade	ed until		the	
		COU	count value is written (one or two bytes										
		dep	depending on the mode selected by the RL bits).										
	MVI A,05 _h	Lower or	der b	oyte o	f th	ne co	ount	is	s lo	baded i	n	to	
		Accumulat	or as	05 _H .									

	REC	GISTE	RS											
	A ()5 X	Х	F										
	Вγ	XX X	Х	С										
	Dy	XX X	Х	Е										
	Η	XX X	Х	L										
OUT CNTO	Load COU	ITER	0 w	ith	low	er c	orde	r by	yte.					
	HINTS:													
		Орсс	de	use	ed i	for	CNT	. 0.	is	$C\mathcal{B}_{H}$,whi	ch	is	the
		memo	ory .	addı	cess	of	the	Сот	unte	er O	- <i>Ti</i>	mer	8253	•
		Cour	iter	0	of	the	823	53 i	has	bee	n use	ed c	n c	ard
		for the single step function.												
	TIPS:	IPS: I/O ADDRESS OF 8253												
			\mathbf{A}_7	A_6	A_5	A_4	A_3	\mathbf{A}_2	A ₁	\mathbf{A}_0	HEX			
	CONTROL	REG	1	1	0	0	1	1	1	0	CE			
	COUNTER	0	1	1	0	0	1	0	0	0	C8			
	COUNTER	1	1	1	0	0	1	0	1	0	CA			
	COUNTER	2	1	1	0	0	1	1	0	0	CC			
					<u> </u>	Ŭ	<u> </u>	· ·	Ŭ	•				
MVI A,00 _H	Higher d	order	b	yte	of	tl	he	cou	nt	is	load	led	in	to
	Accumulat	tor a	s 0	0 _н .										
	REC	GISTE	RS											
	A ()0 X	Х	F										
	Вγ	XX X	Х	С										
	Dy	XX X	X	E										
	Η	XX X	Х	L										
OUT CNTO	Load COU	ITER	0 w.	ith	hig	her	ord	er k	byte	•.				
	OPERATIO	V:												
	Now the .	16-bi	lt c	oun	t is	10	adec	l in	to	the	cour	nter	and	on
	command,	cour	nter	beg	gins	to	dec	crem	ent	the	coun	t u	ntil	it
	reaches	0.At	the	end	d of	th	e co	ount	, i	t ge	nerat	es a	a pu.	lse
	that can	be ı	ised	to	int	errı	ıpt	the	mic	rop	roces	sor.		
HLT	The MPU	fini	shes	ex	ecut	ting	th	e_c	urre	ent	instr	ucti	on a	and
	halts an	y tu	rthe	er (exec	uti	on.	The	e M∃ ∙⊥	20 €	enters	s th	e Ha	alt
	Acknowled	dge n	nach	ıne	сус	:⊥e	and	Wai	it s	stat	es ar	e i	nser	ted
	in every	CTOC	кр	eric	ba.	The	ado	ires	s ar	na t	ne da	ta k	ous a	are
	placed 1	n the	e ni	.gn	⊥mpe	eαan ≠ad	ce	stat	_e.	Tune	cont	ent	OI 1	une Nr
	registers	s ar - ia	e i	unai	rec	tea to f	au.	rinc f~	j t ∽m ∸	ne be '	нцт. тај+	sta a+a+	ce.	An
	Incerrupt	S	nec	2552	ιſΥ	LO E	コエスミ	IIC	σπ τ	.ne i	nd⊥t ¦	slat	е.	



PROGRAMMABLE ONE SHOT

ALGORITHM

1.After loading the counter, the output remains low following the rising edge of the gate input.

2. The output will go high on terminal count.

3.It is Re-triggerable, hence the output will remain low for the full count after any rising edge of the gate input.

ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4200		MVI A,32 _H	3E 32
4202		OUT CWR	D3 CE
4204		MVI A,05 _h	3E 05
4206		OUT CNTO	D3 C8
4208		MVI A,00 _H	3E 00
420A		OUT CNTO	D3 C8
420C		OUT DO	D3 D0
420E		HLT	76

LABEL	MNEMONICS		DESCRIPTION										
	MVI $A, 32_{H}$	Initializ	ing the	e COUN	TER O	of t	he P	IT 83	253	in MODE 1	. by		
		writing th	he con	trol w	ord as	з 32 _н .							
		COMMENT	SELEC	Т	READ	/	M	IODE		BCD/			
			COUNT	ER	LOAD					BINARY			
			SC1	SC0	RL1	RL0	М2	M1	M0	COUNT			
		DATA	D ₇	D ₆	D_5	D ₄	D ₃	D_2	D_1	D ₀			
		BITS	0	0	1	1	0	0	1	0			
		OBSERVE	COUN	NTER	LSB/	MSB	Μ	ODE	1	BINARY			
				D						COUNT			
				_									
		32. is mov	is moved to accumulator										
		REG	ISTERS	accuna	14001	•							
		A 32	2 XX	F									
		B XX	X XX	С									
		D XX	XX X	Е									
		H XX	XX X	L									
	OUT CWR	Write the	contro	ol wor	d in t	the co	ontro	ol re	egist	cer.			
	MVI A,05 _H	Lower or	der b	yte c	of th	ne co	ount	is	108	aded in	to		
		Accumulate	or as I	05 _H .									
		DEC											
			A 05 XX F										
		B V		C									
		D V		Ē									
		H XX		L									

OUT CNTO	Load COUNTER 0 wit	th lower order byte.										
	<u>HINT:</u>											
	U Opcode used	for $CNTO$ is $C8_H$, which	ch is the memory									
	address of t	the Counter 0 - Timer 8	8253.									
MVI A,00 _H	Higher order by	te of the count is	loaded in to									
	Accumulator as $00_{\rm H}$	1 •										
	REGISTERS											
	A 00 XX F											
	B XX XX C											
	D XX XX E											
	H XX XX L											
OUT CNTO	Load COUNTER 0 wit	th higher order byte.										
OUT DO	To trigger GATE 0	trigger GATE 0 of the Counter 0.										
	The GATE inputs	of 8253 are pulled	l high by 3.3k									
	resistors. GATE	0 is also connected	to pin 13 of									
	74LS138. This pro	ovision has been given	n to trigger the									
	GATE											
	TIPS:											
	➢ GATE signal	is the input signal to	o the counter.									
	➢ GATE signal	l of the counter is	used either to									
	enable or di	isable counting.										
	➢ GATE SETTING	g of a counter										
	MODE LOW OR	RISING	HIGH									
	GOING LOW											
	1 –	(1) Initiates counting	-									
		(2)Resets output										
		after next clock										
HLT	Execution of the p	processor is stopped.										

OUTPUT WAVEFORM



BAUD RATE GENERATOR

ALGORITHM

1.It is a simple divide by N counter.

2. The output will be low for one period of clock input.

3. The period from one input pulse to the next equals the number of input counts in the count register.

4.If the count register is reloaded between output pulses, the present period will not be affected but the subsequent period will reflect the new value.

ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4300		MVI A,74 _H	3E 74
4302		OUT CWR	D3 CE
4304		MVI A,0A _H	3E 0A
4306		OUT CNT1	D3 CA
4308		MVI A,00 _H	3E 00
430A		OUT CNT1	D3 CA
430C		HLT	76

LABEL	MNEMONICS		DESCRIPTION										
	MVI A,74 _H	Initializi	nitializing the COUNTER 1 of the PIT 8253 in MODE 2 by										
		writing th	riting the control word as $74_{_{ m H}}$.										
											_		
		COMMENT	SELEC	Т	READ)/	MODE			BCD/			
			COUNTER I)				BINARY			
			SC1 SC0 F			RL0	M2	M1	M0	COUNT			
		DATA	TA D_7 D_6			D ₄	D ₃	D_2	D_1	D ₀			
		BITS	0	1	1	1	0	1	0	0			
		OBSERVE	COUN	ITER	LSB/	MSB	Μ	ODE	2	BINARY			
			1					-		COUNT			
		74. is move	ed to	accum	ulato	١r]		
		REGI	ISTERS	a coun	uruce	•							
		A 74	I XX	F									
		B XX		С									
		D XX		Е									
		H XX		L									
	OUT CWR	Write the	contr	col wo	rd in	the	cont	crol	reg	ister.			
	MVI $A, 0A_{H}$	Lower or	der 1	byte	of	the	cour	nt	is	loaded	in	to	
		Accumulato	or as	OA_{H} .									
		REGI	ISTERS	5									
		A OA	A XX	F									
		B XX	XX	С									
		D XX	XX X	E									
		H XX	XX	L									
						-							
	OUT CNT1	Load COUNT	rer 1	with	lower	orde	er by	yte.					

	 HINT: Opcode used for CNT1 is CA_H, which is the memory address of the Counter 1 - Timer 8253. Counter 1 of the 8253 has been used on card for generation of the TXD and RXD baud clock required by USART (8251A).
MVI A,00 _H	Higher order byte of the count is loaded in to Accumulator as 00_{H} . REGISTERS A 00 XX F B XX XX C D XX XX E H XX XX L H
OUT CNT1	Load COUNTER 1 with higher order byte.
HLT	Execution of the processor is stopped.

OUTPUT WAVEFORM



SQUARE WAVE GENERATOR

ALGORITHM

1. It is similar to mode2 except that the output will remain high until one half of the count and go low for other half for even number count.

2. If the count is odd the output will be high for $(\operatorname{count} +1)/2$ counts and low for $(\operatorname{count} -1)/2$ counts.

3. This mode is the mode for generating baud rate for 8251A(USART).

ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4400		MVI A,36 _h	3E 36
4402		OUT CWR	D3 CE
4404		MVI A,0A _H	3E 0A
4406		OUT CNTO	D3 C8
4408		MVI A,00 _H	3E 00
440A		OUT CNTO	D3 C8
440C		HLT	76

LABEL	MNEMONICS		DESCRIPTION										
	MVI A,36 _H	Initializ	nitializing the COUNTER 0 of the PIT 8253 in MODE 3 by										
		writing t	riting the control word as 36_{H} .										
					-								
		COMMENT	SELEC	Т	READ)/	M	IODE		BCD/			
			COUNT	'ER	LOAD)				BINARY			
			SC1	SC0	RL1	RL0	M2	M1	M0	COUNT			
		DATA	D ₇	D ₇ D ₆		D ₄	D ₃	D ₂	D_1	D ₀			
		BITS	0	0	1	1	0	1	1	0			
		OBSERVE	COUN	ITER	LSB/	MSB	Μ	ODE	Ξ3	BINARY			
			C)						COUNT			
			-	•									
		36 _H is mov	ved to	accum	ulato	or.							
		REG	REGISTERS										
		A 3	6 XX	F									
		ВХ	X XX	С									
		D X	X XX	Е									
		Н Х	X XX	L									
	OUT CWR	Write the	e cont	rol w	ord i	n to	the	e co	ntro	l regist	er a	nd	
		the coun	it to	chan	nel0	so	that	с ус	ou q	get an	outp	ut	
		frequency	r of 15	ōKHz w	hose	input	clo	ock	is n	early 1.	5MHz	•	
	MVI A, OA _H	Lower or	der 1	byte	of	the	cour	nt	is	loaded	in	to	
		Accumulat	ccumulator as OA _H .										
		REG	ISTERS	5 									
		A 0	A XX	F C									
			X XX	С Б									
			X XX	T.									
		п Х	X XX	Ц									

OUT CNTO	Load COUNTER 0 with lower order byte.							
MVI A,00 _H	Higher order byte of the count is loaded in to Accumulator as $\rm OO_{H}.$							
	REGISTERSA 00 XX FB XX XX CD XX XX EH XX XX L							
OUT CNTO	Load COUNTER 0 with higher order byte. <u>OPERATION:</u> Now the 16-bit count is loaded in to the counter and on command, counter begins to decrement the count until it reaches 0.At the end of the count, it generates a pulse that can be used to interrupt the microprocessor.							
HLT	Execution of the processor is stopped.							



HARDWARE TRIGGERED MODE

ALGORITHM

1. The counter starts counting after rising edge of trigger input and output goes low for one clock period when terminal count is reached.

2. Counter is Re-triggerable.

3. After 6th pulse, initially high output goes low and half on next pulse.

ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4500		MVI A,1A _H	3E 1A
4502		OUT CWR	D3 CE
4504		MVI A,05 _h	3E 05
4506		OUT CNTO	D3 C8
4508		OUT DO	D3 D0
450A		HLT	76

LABEL	MNEMONICS	DESCRIPTION										
	MVI A,1A _H	Initializ	ing tl	he cou	NTER	0 of	the	PII	: 825	53 in MO	DE 5	by
		writing the control word as $1A_{H}$.										
											_	
		COMMENT	COMMENT SELECT		READ)/	MODE			BCD/		
			COUNTER		LOAD)				BINARY		
			SC1	SC0	RL1	RL0	M2	M1	M0	COUNT		
		DATA	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D_1	D ₀		
		BITS	0	0	0	1	1	0	1	0		
		OBSERVE	COUN	NTER	LS	SB	Μ	ODE	Ξ5	BINARY		
				D						COUNT		
				-							1	
		1A _H is mov	ved to	accum	nulato	or.						
		REG	ISTER	S								
		A 1	A XX	F								
		ВХ	X XX	С								
		D X	X XX	Е								
		Н Х	X XX	L								
	OUT CWR	Write the	e conti	rol wo	rd in	1 the	cont	trol	reg	ister.		
	MVI A,05 _h	Lower order byte of the count is loaded in						in	to			
		Accumulat	or as	05 _H .								
		DEC		~								
		REG	FISTER:	5 1 m								
			5 XX	r C								
			X XX	С Т								
			X XX	т.								
		11 X	X XX	<u> </u>	1		1					
	OUT CNTO	Load COUN	TER 0	with	Lower	orde	er b <u>r</u>	yte.				
		To training	~~~~		+ h c	Court	/	2				
	DOL DO	TO TRIGGE	er GATI	L V OI	τne	count	ler (J.				







REFERENCE

- 1. Ramesh S.Gaonkar, Microprocessor Architecture, Programming, and Applications, Fourth Edition, Penram International Publishing (India), 2000.
- 2. S.Subathra, "Advanced Microprocessor Laboratory", Record work, Adhiparashakthi Engineering College, Melmaruvathur, October 2002
- 3. S.Subathra, "Programming in 8085 Microprocessor and its applications An Innovative Analysis", Technical Report, March 2003
- 4. Micro-85 EB, User Manual, Version 3.0, CAT #M85 EB-002, VI Microsystems Pvt. Ltd., Chennai.