INTERFACING USING PIC

BY

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OBJECTIVE

To write and assembly language program to interface PIC with 8085 Microprocessor kit

APPARATUS REQUIRED

- 8085 Microprocessor kit
- PIC kit
- Power supply
- Flat Ribbon Cable

ALGORITHM

1. Input the command word to the accumulator
2. Out it through ICW and OCW registers in R/W logic suitably
3. Write all the ICW's required in the command registers and also occurs
4. At the interrupt vector location, use RST1, so that the system is reset to indicate the execution of ISR

INITIALISATION MODE

To initialize 8259 with following specifications,

1.ICW4 needed single 8259.
2.Interval of 4, edge triggered mode, A7, A6, A5 = 000
3.Interrupt service routine address for IRO is 5000H
4.8085 mode normal EOI, non-buffer mode, not specially fully nested mode, mask all the interrupt except IRO

VERIFICATION

If you press switch IRO ,the CPU jumps to location 5000H .8259 will not accept any more interrupts at IR0, since AEOI is not set, then EOI is given through OCW2.

SPECIAL MASK MODE

VERIFICATION

Press the switch IR0, CPU jumps to 5000H, and execute a program there, normally since no EOI command is given 8259 will not accept further interrupts, however due to special mask mode 8259, will accept interrupt only at IR1,since only IR1, is enabled at that location.

INITIALISATION COMMAND WORD FOR 8259

ICW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
D_0	A_7	A_6	A_5	1	LTM	AD1	SNGL	IC4

If D_1 = 1, single mode
D_1 = 0, single mode
If D_2 = 1, call address interval of 4
D_2 = 0, call address interval of 8
If D_3 = 1, level triggered mode
D_3 = 0, edge triggered mode
If D_0 = 1, ICW4 is needed
D_0 = 0, ICW4 is not needed
A_7 ,A_6 ,A_5 interrupt vector address

ICW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

Where A_8 to A_{15} → interrupt vector address

ICW4

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SNFM	BUF	M/S	AEOI	MDM

If D_1 = 0, auto EOI
D_1 = 1, normal EOI
If D_0 = 1, 8086
D_0 = 0, 8080/85
If SNFM=1,specially fully nested mode
SNFM=0,specially fully nested mode

D_3	D_2	
0	X	Non buffered mode
1	0	Buffered mode/slave
1	1	Buffered mode/master

OPERATIONAL COMMAND WORD FOR 8259

OCW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0

if the bits are 1,then mask is set , if they are 0, then mask is reset.

OCW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	R	SL	EOI	0	0	L_2	L_1	L_0

For L_2, L_1, L_0 IC IR lever lobe acted upon 76543210

D_7	D_6	D_5	
0	0	1	Non specific EOI command
0	1	1	Specific EOI
1	0	1	Rotate on non specific EOI command
1	0	0	Rotate in automatic EOI command
0	0	0	Rotate in automatic rotation
1	1	1	Rotate specific EOI command
1	1	0	Set priority command
0	1	0	No operation

OCW3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	ESMM	SMM	0	1	P	PR	RTS

If D_2 = 1, no poll command
D_2 = 0, poll command

ESMM	SMM	
0	0	No operation
0	1	
1	0	Reset special mask
1	1	Set special mask

PR	RTS	
0	0	No action
0	1	
1	0	Read ISR ON RD pulse
1	1	Read ISR ON RD pulse

Initialisation Mode

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND	COMMENT
4000		**MVI A,17** $_H$	3E 17	Initialize 8259 in single mode.
4002		**OUT C0** $_H$	D3 C0	Port address for ICW1.
4004		**MVI A,50** $_H$	3E 50	Higher order address
4006		**OUT C2** $_H$	D3 C2	Port address for ICW2.
4008		**MVI A,00** $_H$	3E 00	Lower order address
400A		**OUT C2** $_H$	D3 C2	Port address for ICW4
400C		**MVI A,FE** $_H$	3E FE	Mask is set to interrupt except IR0
400E		**OUT C2** $_H$	D3 C2	Port address for OCW1
4010		**HLT**	76	Stop the execution
5000		**MVI A,20** $_H$	3E 20	To specify non specific EOI

				command
5002		**OUT C0** $_H$	D3 C0	Out it through OCW2
5004		**RST 1**	C7	Set the RST1 interrupt

Special Mask Mode

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND	COMMENT
4500		**MVI A,17** $_H$	3E 17	Set 8259 in single mode
4502		**OUT C0** $_H$	D3 C0	Port address for ICW1
4504		**MVI A,50** $_H$	3E 50	Load the higher order address in accumulator
4506		**OUT C2** $_H$	D3 C2	Out the data through ICW2
4508		**MVI A,00** $_H$	3E 00	Load the lower order address in accumulator
450A		**OUT C2** $_H$	D3 C2	Out the data through ICW4
450C		**MVI A,00** $_H$	3E 00	Load the accumulator with the data . Set the interrupts.
450E		**OUT C2** $_H$	D3 C2	Out the data through OCW1
4510		**MVI A,68** $_H$	3E 68	The data to be display before interrupts
4512		**OUT C2** $_H$	D3 C2	Out the data through port address
4514		**HLT**	76	Stop the execution
5000		**MVI A,FD** $_H$	3E FD	The data to be displayed after pressing interrupt
5002		**OUT C2** $_H$	D3 C2	Out the data
5004		**RST 1**	C7	Set the RST1 interrupt

Execution

Initialisation Mode

In this if IR0 is pressed then the control jumps to 5000H and executes to display 20H. Further any interrupt is not accepted.

Special Mask Mode

In this IR0,IR1 is enabled then control jumps to 5000H and executes to display FDH . If IR1 is pressed after the IR0 then ‘50’ is displayed.

REFERENCE

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2. S.Subathra, “Programming in 8085 Microprocessor and its applications – An Innovative Analysis”, Technical Report, Adhiparashakthi Engineering College, Melmaruvathur, March 2003