DMA TRANSFER

BY

SUBATHRA S

DMA TRANSFER

OBJECTIVE

To initialize 8237 for read, write and memory to memory transfer mode.

READ TRANSFER MODE

Specification

- Channel 0
- Address hold disable
- Auto initialize disable
- Address increment select
- Block transfer mode
- Software address

Procedure

1. Reset the program.
2. Read the program.
3. Enter program in user RAM area.
4. This program will load and initialize internal register of 0237.
5. Enter the status program for another user RAM area.
6. This program will input the status of 8237 after the transfer is over.
7. Store the status starting from memory location 4300 H.
8. For the CPU, the local memory is mapped at C000H to DFFFH execute program1 followed by program2.

WRITE TRANSFER MODE

Specification

- Write transfer
- Auto initialize disable
- Address increment select
- Block transfer mode
- Software request
- Channel 0

Procedure

1. Enter write transfer program at user RAM area
2. This program will initialize the base address, word count mode and mask register
3. Enter the status mode from another user RAM. This program will input the status of 8237 after write transfer is over
4. Set all the bits in a 8 bit DIP switch mode, till the DMA transfer buffer memory with the known data say FFH.

MEMORY TO MEMORY TRANSFER MODE

Specification

- Channel 0
- Address hold disable

- Auto initialize disable
- Address 0 increment select
- Software request

Procedure

1. Enter the program to load the base and current address and word count register of channel 0 and 1
2. Enter the program at different memory location for loading the command mode and mask register
3. Fill the memory from C000 to C005 and D000 to D005 as follows,

   C000 – 00 D000 - 00
   C001 – 01 D001 - 00
   C002 – 02 D002 - 00
   C003 – 03 D003 - 00
   C004 – 04 D004 - 00
   C005 – 05 D005 - 00

   execute program1 followed by program2.

ASSEMBLY LANGUAGE PROGRAM MEMORY TO MEMORY TRANSFER

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4100		**OUT DA_H**	D3 DA
4102		**OUT $D8_H$**	D3 D8
4104		**MVI A,00_H**	3E 00
4106		**OUT $C0_H$**	D3 C0
4108		**MVI A,00_H**	3E 00
410A		**OUT $C0_H$**	D3 C0
410C		**OUT $D8_H$**	D3 D8
410E		**MVI A,05_H**	3E 05
4110		**OUT $C2_H$**	D3 C2
4112		**MVI A,00_H**	3E 00
4114		**OUT $C2_H$**	D3 C2
4116		**OUT $D8_H$**	D3 D8
4118		**MVI A,00_H**	3E 00
411A		**OUT $C4_H$**	D3 C4
411C		**MVI A,10_H**	3E 10
411E		**OUT $C4_H$**	D3 C4
4120		**OUT $D8_H$**	D3 D8
4122		**MVI A,05_H**	3E 05
4124		**OUT $C6_H$**	D3 C6
4126		**MVI A,00_H**	3E 00
4128		**OUT $C6_H$**	D3 C6
412A		**RST 1**	CF
4200		**MVI A,01_H**	3E 01
4202		**OUT $D0_H$**	D3 D0
4204		**MVI A,88_H**	3E 88
4206		**OUT D6 $_H$**	D3 D6
4208		**MVI A,85_H**	3E 85
420A		**OUT $D6_H$**	D3 D6
420C		**MVI A,$0E_H$**	3E 0E

420E		**OUT DE_H**	D3 DE
4210		**MVI A,04_H**	3E 04
4212		**OUT $D2_H$**	D3 D2
4214		**RST 1**	CF

WRITE TRANSFER

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4100		**OUT DA_H**	D3 DA
4102		**OUT $D8_H$**	D3 D8
4104		**MVI A,00_H**	3E 00
4106		**OUT $C0_H$**	D3 C0
4108		**MVI A,00_H**	3E 00
410A		**OUT $C0_H$**	D3 C0
410C		**OUT $D8_H$**	D3 D8
410E		**MVI A,05_H**	3E 05
4110		**OUT $C2_H$**	D3 C2
4112		**MVI A,00_H**	3E 00
4114		**OUT $C2_H$**	D3 C2
4116		**OUT $D8_H$**	D3 D8
4118		**MVI A,00_H**	3E 00
411A		**OUT $D0_H$**	D3 D0
411C		**MVI A,84_H**	3E 84
411E		**OUT $D6_H$**	D3 D6
4120		**MVI A,$0E_H$**	3E 0E
4122		**OUT DE_H**	D3 DE
4124		**MVI A,04_H**	3E 04
4126		**OUT $D2_H$**	D3 D2
4128		**RST 1**	CF

TRANSFER CHECK

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4100		**OUT DA_H**	D3 DA
4102		**OUT $D8_H$**	D3 D8
4104		**MVI A,00_H**	3E 00
4106		**OUT $C0_H$**	D3 C0
4108		**MVI A,00_H**	3E 00
410A		**OUT $C0_H$**	D3 C0
410C		**OUT $D8_H$**	D3 D8
410E		**MVI A,05_H**	3E 05
4110		**OUT $C2_H$**	D3 C2
4112		**MVI A,00_H**	3E 00
4114		**OUT $C2_H$**	D3 C2
4116		**OUT $D8_H$**	D3 D8
4118		**MVI A,00_H**	3E 00
411A		**OUT $D0_H$**	D3 D0
411C		**MVI A,88_H**	3E 88
411E		**OUT $D6_H$**	D3 D6
4120		**MVI A,00_H**	3E 00
4122		**OUT $D4_H$**	D3 D4
4124		**MVI A,04_H**	3E 04
4126		**OUT $D2_H$**	D3 D2
4128		**RST 1_H**	CF

STATUS CHECK

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
4200		**LXI H,4300$_H$**	21 00 43
4204		**OUT D8$_H$**	D3 D8
4206		**IN C0$_H$**	DB C0
4208		**MOV M,A**	77
4209		**INX H**	23
420A		**IN C0$_H$**	DB C0
420C		**MOV M,A**	77
420D		**INX H**	23
420E		**OUT D8$_H$**	D3 D8
4210		**IN C2$_H$**	DB C2
4212		**MOV M,A**	77
4213		**INX H**	23
4214		**IN D0$_H$**	DB D0
4216		**MOV M,A**	77
4217		**RST 1**	CF

EXECUTION
MEMORY TO MEMORY TRANSFER

MODE	ADDRESS	DATA
INPUT	C000	00_H
	C001	01_H
	C002	02_H
	C003	03_H
	C004	04_H
	C005	05_H
	D000	00_H
	D001	00_H
	D002	00_H
	D003	00_H
	D004	00_H
	D005	00_H
OUTPUT	C000	00_H
	C001	01_H
	C002	02_H
	C003	03_H
	C004	04_H
	C005	05_H
	D000	00_H
	D001	01_H
	D002	02_H
	D003	03_H
	D004	04_H
	D005	05_H

WRITE TRANSFER

MODE	ADDRESS	DATA
INPUT	C000	FF_H
	C001	FF_H
	C002	FF_H
	C003	FF_H
	C004	FF_H
	C005	FF_H
OUTPUT	C000	00_H
	C001	00_H
	C002	00_H
	C003	00_H
	C004	00_H
	C005	00_H

TRANSFER CHECK

MODE	ADDRESS	DATA
INPUT	C000	00_H
	C001	01_H
	C002	02_H
	C003	03_H
	C004	04_H
	C005	05_H
OUTPUT	C000	05_H IS DISPLAYED IN LED
	C001	
	C002	
	C003	
	C004	
	C005	

STATUS CHECK

MODE	ADDRESS	DATA
OUTPUT	4300	06_H
	4301	01_H
	4302	FF_H

REFERENCE

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2. S.Subathra, “Programming in 8085 Microprocessor and its applications – An Innovative Analysis”, Technical Report, Adhiparashakthi Engineering College, Melmaruvathur, March 2003