ADC SUCCESSIVE APPROXIMATION METHOD



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ADC - SUCCESSIVE APPROXIMATION METHOD

OBJECTIVE

To perform analog to digital conversion by interfacing Analog to Digital Convertor with 8085 Microprocessor using Successive Approximation Method.

APPARATUS REQUIRED

- 8085 Microprocessor Trainer kit
- Successive Approximation ADC (ALS-NIFC-07) Kit
- Power Supply
- RPS (0 5v)
- Flat Ribbon Cable

DESCRIPTION

The ADC interface consists of a NOR gate crystal oscillator, a CMOS clock driver which feeds 768Khz as the input clock to the ADC, a regulator (723) to connect the +12v to +5v required by the IC, a stable voltage reference(LM 336) and buffer (which provides +5v reference). A multi turn cermet allows adjustment to the reference voltage.

The channel select, ALE, start conversion and output enable lines are interfaced through port lines (connect a flat cable from the programmable peripheral interface 8255 connector on the trainer to the connector C_1 in the interface).

PORT LINES	DESCRIPTION
PA ₀ - PA ₇	Connect data line D ₀ - D ₇
PB ₀	Channel select data lines A
PB ₁	Channel select line B
PB ₂	Channel select line C
PB ₅	ALE to latch the address
PB ₆	Start conversion
PB ₇	Input Enable
PC ₀	End of conversion

ALGORITHM

- Initialize the 8255 PPI in I/O operation.
- Give start of conversion by making PB6 high transition.
- PB7 is made high during the digital value.
- The digital value is sent to Port A and the digital value is displayed.

BLOCK DIAGRAM

NIFC 07

8 BIT SUCCESSIVE APPROXIMATION ADC INTERFACE



PORT BITS PA0 - PA7

ALL PORT BITS ARE TERMINATED IN A CONNECTOR P4

ASSEMBLY LANGUAGE PROGRAM

ADDRESS	LABEL	MNEMONICS	OPCODE/OPERAND
C200		MVI A,91 _H	3E 91
C202		OUT CWR	D3 DB
C204	NEXT	MVI A,60 _H	3E 60
C206		OUT PORTB	D3 D9
C208		XRA A	AF
C209		OUT PORTB	D3 D9
C20B		MVI A,80 _H	3E 80
C20D		OUT PORTB	D3 D9
C20F		MVI A,EO _H	3E E0
C211		OUT PORTB	D3 D9
C213	REPEAT	IN PORTC	DB DA
C215		RRC	OF
C216		JC REAPEAT	DA 13 C2
C219		MVI A,60 _H	3E 60
C21B		OUT PORTB	D3 D9
C21D		IN PORTA	DB D8
C21F		STA FFF9 _H	32 F9 FF
C222		CALL UPDDT	CD D3 06
C225		JMP NEXT	C3 04 C2

LABEL	MNEMONICS	DESCRIPTION								
	MVI A,91 _H	Initializ	Initializing the ports of the PPI 8255 as O/P ports by			orts by				
		writing t	he cor	ntro	l wo	ord as 9	91 _H .			
		*								
		DATA	D7	D ₆	D_5	D ₄	D ₃	D_2	D_1	D ₀
		BITS	1	0	0	1	0	0	0	1
		COMMENT	I/O	Мос	le0	PortA	PortC	Mode0	PortB	PortC
			mode			I/P	Upper		O/P	Lower
							O/P			I/P
		$91_{\rm H}$ is mov	ved to	acc	umu	lator.				
		REC	REGISTERS							
		A 9	1 XX	F						
		ВХ	X XX	С						
		DX	X XX	E						
		Н Х	X XX	L						
		Control v	ord s	neci	fio	e +ho 1	[/O fun	ation f	for eacl	norte
		of 8255	VOIU 3	рест	TTE	5 CHE 1	L/O LUIN		OI Caci	i ports
NEXT	MVI A,60	60. is lo	aded i	n to	b th	e Accum	ulator.			
		00H 10 10	OUH IS IOAded IN LO LHE ACCUMULATOR.							
		REG	ISTER	5						
		A 6	$\mathbf{A} \begin{bmatrix} 60 \\ XX \end{bmatrix} \mathbf{F}$							
		$B \xrightarrow{\mathbf{c}} \mathbf{A} \xrightarrow{\mathbf{c}} \mathbf{c}$								
		D XX XX E								
		H XX XX L								
				1						
		✤ DEFAULT OE SELECTION								
		Since the OE, START & ALE were connected to								
		Port	Bof	PPI	bit	ts B ₇ , 1	B ₆ , B ₅ t	hrough	an in	verter.
		Hence if we give '0' as input, it will be								
		complemented & the output 'l' is being generated at								
		the other end.								
		המיקמ	в	B	Г	R B	BB	BB		
		BITS	0	1 1	1	1 0	0 0	D ₁ D ₀		
		COMMENT	OES	- TAR1	ים י			B A		
	OUT PORTB	Output th	e 60.	conf	iau	ration	through	port F	3	
	XRA A	Clear the		nula	tor.		enrougn	Porer	•	
		REG	ISTER	5	001					
		A 0	0 XX	F						
		B X	x xx	С						
		D X	X XX	Е						
		H V	X XX	L						
				J						
	OUT PORTB	Output th	100 H	conf	Eigu	ration	through	n Port I	З.	

	MVI A,80 _H	$80_{\rm H}$ is loaded in to Accumulator.		
		REGISTERS		
		A 80 XX F		
		B XX XX C		
		D XX XX E		
		H XX XX L		
		•		
		* START CONVERSION		
		In order to start conversion, we set bit		
		START & ALE low and OE high initially. During		
		nardware process, it will be complemented & output		
		13 processed.		
		DATA B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0		
		$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		
		COMMENT OE START ALE X C B A		
	OUT PORTB	Output the 80_{H} configuration through Port B.		
	MVI A,E0 _H	EO _H is moved to accumulator.		
		REGISTERS		
		A EO XX F		
		B XX XX C		
		H XX XX L		
		• DISABLE START, ALE, OF		
		Initially set START, ALE, OE high Hence in		
		the hardware process, it will be complemented & they		
		are disabled.		
		DATA B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0		
		BITS 1 0 0 0 0 0 0 0		
		COMMENT OE START ALE X C B A		
	OUT PORTB	Output the EO_H configuration through Port B.		
REPEAT	IN PORTC	Read data ready status.		
		Since Port C lower bits are configured as input bits		
		$(PC_3 - PC_0)$		
	DDC	$(PC_3 - PC_0)$		
1	RRC	(PC ₃ -PC ₀) Rotate D ₀ into carry flag.		
	RRC JC BEADEAU	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check</pre>		
	RRC JC REAPEAT	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60, is loaded in to Accumulator.</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator.</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator. REGISTERS</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator. REGISTERS A 60 XX F</pre>		
	RRC JC REAPEAT MVI A,60 _H	$(PC_{3} -PC_{0})$ Rotate D ₀ into carry flag. If D ₀ =1, conversion is not yet complete; go back & check. 60_{H} is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C		
	RRC JC REAPEAT MVI A,60 _H	$(PC_{3} -PC_{0})$ Rotate D ₀ into carry flag. If D ₀ =1, conversion is not yet complete; go back & check. $60_{H} \text{ is loaded in to Accumulator.}$ $\textbf{REGISTERS}$ $\textbf{A} 60 XX F \\ B XX XX C \\ D XX XX E \\ \end{tabular}$		
	RRC JC REAPEAT MVI A,60 _H	$(PC_{3} -PC_{0})$ Rotate D ₀ into carry flag. If D ₀ =1, conversion is not yet complete; go back & check. $60_{H} \text{ is loaded in to Accumulator.}$ $\begin{array}{c c} \textbf{REGISTERS} \\ \textbf{A} & \textbf{60} & XX & F \\ B & XX & XX & C \\ D & XX & XX & E \\ H & XX & XX & L \end{array}$		
	RRC JC REAPEAT MVI A,60 _H	$(PC_{3} -PC_{0})$ Rotate D ₀ into carry flag. If D ₀ =1, conversion is not yet complete; go back & check. $60_{H} \text{ is loaded in to Accumulator.}$ $\textbf{REGISTERS}$ $\textbf{A} 60 XX F \\ B XX XX C \\ D XX XX E \\ H XX XX L \\ \textbf{H}$		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C D XX XX E H XX XX L</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C D XX XX E H XX XX E H XX XX L * DEFAULT OE SELECTION Since the OE, START, ALE are connected to Port</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C D XX XX E H XX XX L * DEFAULT OE SELECTION Since the OE, START, ALE are connected to Port B of PPI bits B₇, B₆, B₅ through an inverter. Hence if</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C D XX XX E H XX XX L * DEFAULT OE SELECTION Since the OE, START, ALE are connected to Port B of PPI bits B₇, B₆, B₅ through an inverter. Hence if we give '0' as input, it will be complemented & the</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C D XX XX E H XX XX E H XX XX L C DEFAULT OE SELECTION Since the OE, START, ALE are connected to Port B of PPI bits B₇, B₆, B₅ through an inverter. Hence if we give '0' as input, it will be complemented & the output '1' is being generated at the other end.</pre>		
	RRC JC REAPEAT MVI A,60 _H	<pre>(PC₃ -PC₀) Rotate D₀ into carry flag. If D₀ =1, conversion is not yet complete; go back & check. 60_H is loaded in to Accumulator.</pre>		
	RRC JC REAPEAT MVI A,60 _H	$(PC_{3} - PC_{0})$ Rotate D ₀ into carry flag. If D ₀ =1, conversion is not yet complete; go back & check. 60_{H} is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C D XX XX E H XX XX E H XX XX L C D Since the OE, START, ALE are connected to Port B of PPI bits B ₇ , B ₆ , B ₅ through an inverter. Hence if we give '0' as input, it will be complemented & the output '1' is being generated at the other end. DATA B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀ PATA B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀		
	RRC JC REAPEAT MVI A,60 _H	$(PC_{3} - PC_{0})$ Rotate D ₀ into carry flag. If D ₀ =1, conversion is not yet complete; go back & check. 60_{H} is loaded in to Accumulator. REGISTERS A 60 XX F B XX XX C D XX XX E H XX XX L * DEFAULT OE SELECTION Since the OE, START, ALE are connected to Port B of PPI bits B ₇ , B ₆ , B ₅ through an inverter. Hence if we give '0' as input, it will be complemented & the output '1' is being generated at the other end. DATA B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀ BITS O 1 1 0 0 0 0 0		
	RRC JC REAPEAT MVI A,60 _H	$(PC_{3} - PC_{0})$ Rotate D ₀ into carry flag. If D ₀ =1, conversion is not yet complete; go back & check. 60 _H is loaded in to Accumulator. REGISTERS A 60 XX B XX XX C D XX XX H XX XX C D XX XX H XX XX L C D EFAULT OE SELECTION Since the OE, START, ALE are connected to Port B of PPI bits B ₇ , B ₆ , B ₅ through an inverter. Hence if we give '0' as input, it will be complemented & the output '1' is being generated at the other end. DATA B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀ BITS 0 1 1 0 0 0 0 0 COMMENT OE START ALE X C B A		

IN PORTA	Read output & save it in to the accumulator.			
STA FFF $9_{\rm H}$	Store the result at data field using monitor routine			
	location address.			
CALL	Display at data location.			
UPDDT				
JMP NEXT	Repeat the looping.			

EXECUTION

ANALOG	DIGITAL	
INPUT	OUTPUT	
(volts)	(hexa decimal)	
0.0	00 _H	
0.5	08 _H	
1.0	23 _H	
1.5	3D _H	
2.0	54 _H	
2.5	75 _H	
3.0	93 _H	
3.5	A8 _H	
4.0	C2 _H	
4.5	E2 _H	
5.0	FF	

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